REMARKS

The Office Action (1) rejected claims 12, 13, 16-19, 22, 23, 25 and 27-30 under 35 U.S.C. 102(e) as being anticipated by Yu (US 6,475, 869 B1), (2) rejected claims 14 and 15 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Cheng et al. (US 6,737,670 B2), (3) rejected claim 20 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Assaderaghi et al. (US 6,432,754 B1), (4) rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Gambino et al. (US 6,689,650 B2) and Literature Digest ("The Highlights of IEDM 2002", vol. 6, March 2003, pp. 1-6), and (5) rejected claims 24 and 26 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Bae et al. (US 6,633,066 B1).

1. Regarding claims 12, 13, 16-19, 22, 23, 25 and 27-30 under 35 U.S.C. 102(e) as being anticipated by Yu (US 6,475, 869 B1), applicants have modified independent claim 12, from which claims 13 through 30 depend, to overcome the Examiner's rejection.

Applicants submit that Yu cites the well-known fact that tensile strained silicon region can have higher carrier mobility than conventional silicon channel regions (Col. 2, lines 26-27), and that Yu discloses a finFET

design having SiGe channel material. However, SiGe channel finFET design is not the focus of the present invention.

The present invention discloses a finFET design having a silicon channel and, specifically, a tensile strained finFET design having a silicon channel deposited on a SiGe seed layer. Silicon channel finFET design is not taught by Yu, since Yu only discloses a finFET design having:

- a silicon germanium (SiGe) channel deposited on a substrate (Claims 1, 11 and 18, Col. 4, lines 65-68, Col. 5, lines 1-6, Col. 5, lines 54-55); or

- a silicon germanium channel (SiGe) deposited on a silicon seed layer (Claim 7, Col. 5, lines 60-62).

The basic difference between Yu and the present invention is the channel material. The channel material of Yu is SiGe, either SiGe deposited on a substrate or SiGe deposited on a silicon seed layer. The channel material of the present invention is silicon, deposited on a SiGe seed layer. However, more than just a difference of material, the use of a silicon channel in the present invention provides different strain properties which can lead to device mobility enhancements as compared with SiGe channel devices as in Yu. Therefore, applicants submit that the present invention cannot be anticipated by, nor is there any useful teaching of their claimed invention in Yu.

The strain property of the channel material of Yu is either relaxed SiGe (in the case of SiGe deposited on a substrate), or compressive strained SiGe (in the case of SiGe deposited on a silicon seed layer):

- Relaxed SiGe channel in Yu. When adding germanium to silicon, the silicon in the SiGe compound is under tensile strain since the lattice constant of germanium is larger than that of silicon. However, the

SiGe compound is in equilibrium, meaning it is relaxed and not under any strain at all. Another way to describe it is that in SiGe, silicon is tensile strained and germanium is compressive strained, but the stresses of silicon and germanium balance out so that the SiGe compound is in equilibrium. In other words, the finFET design of Yu has a relaxed SiGe channel with the silicon component being under tensile strain. In certain embodiments of Yu, the SiGe is definitely relaxed because of the additional thermal anneal process (Col. 6, lines 5-11).

- Compressive strained SiGe channel in Yu. When deposited on a silicon seed layer, SiGe is compressively strained since SiGe atoms try to follow the seed silicon lattice (lattice constant of SiGe is larger than that of silicon). Thus, in the embodiment of Yu (SiGe channel on silicon seed), SiGe is under compressive strain. Component-wise, silicon in this compressive SiGe is not under any strain at all (since it follows the lattice of the seed layer, which is also silicon), and germanium is under heavy compressive strain (more than in relaxed SiGe). Compressive strained channel transistors are less desirable as compared to tensile strained channel transistor since the compressive strained channel has enhanced hole mobility but little or no enhanced electron mobility, while tensile strained channels have both enhanced electron and hole mobilities. As mentioned above, the finFET design of Yu has a compressive SiGe channel with the silicon component being relaxed.

In contrast, the strain property of the channel material of the present invention is tensile strained silicon. Using a seed layer of SiGe, the deposited silicon channel layer will extend out to match the lattice constant of SiGe, thus resulting in a tensile strained silicon channel layer in the present invention finFET design. The underlying principle of the present

invention is that the lattice constant of the channel layer (silicon in the above example) has to be smaller than that of the seed layer (SiGe in the above example) so that the channel layer experiences tensile strain. This principle is not disclosed in Yu.

As a variation of the present invention principle, a SiGe channel (lattice constant a) can be deposited on a SiGe seed layer (lattice constant b), provided that $a < b$. To achieve this condition, the germanium content of the channel layer has to be less than that of the seed layer since the lattice constant of SiGe compound is proportionally increased with respect to the concentration of germanium. This variation of the present invention finFET using SiGe channel is also more advantageous than Yu's SiGe channel finFET since the SiGe of the present invention is under tensile strain (because of the larger lattice constant seed layer) as compared to either relaxed or compressive strain SiGe of Yu (because of the anneal process or the smaller lattice constant seed layer).

Applicants submit that Yu does not disclose nor anticipate the deposition of silicon channel on SiGe seed layer as provided by the present invention and specified in amended claim 12. In applicant's invention, the deposition of a silicon channel on a SiGe seed layer (and in general, a channel layer deposited on a seed layer with the lattice constant of the channel layer smaller than that of the seed layer) provides a tensile strained channel finFET design with the achievement of additional improvements in both electrons and holes as compared with the relaxed SiGe or compressive strained SiGe channel finFET disclosed by Yu.

The method specified in amended claim 12 clearly contrasts with any teachings or suggestions in Yu and applicants respectfully submit that, for the reasons set forth above, claim 12 is allowable over Yu. Claims

13, 16-19, 22, 23, 25, and 27-30 all depend from amended claim 12 and contain all the limitations of claim 12 and are allowable for the same reasons as is claim 12.

2. Regarding claims 14 and 15, rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Cheng et al. (US 6,737,670 B2), applicant submits Yu in view of Cheng cannot anticipate and render the claims of the present invention obvious because they do not suggest, teach, or yield a tensile strained channel, achieved by the deposition of a silicon channel layer on a SiGe seed layer. Instead, Yu discloses a SiGe channel layer deposited on a silicon seed layer and Cheng discloses a method to produce relaxed silicon germanium substrate. Cheng in no way solves or cures the omissions of Yu, described in detail above, with regard to producing the tensile strained finFETs of applicant's invention. In addition, claims 14 and 15 depend from claim 12 and contain all the limitations of claim 12 and are allowable for the same reasons as is claim 12.

3. Regarding claim 20 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Assaderaghi et al. (US 6,432,754 B1), applicant submits Yu in view of Assaderaghi et al. cannot anticipate and render the claims of the present invention obvious because they do not suggest, teach, or yield a tensile strained channel, achieved by the deposition of a silicon channel layer on a SiGe seed layer. Instead, Yu discloses a SiGe channel layer deposited on a silicon seed layer and Assaderaghi et al. discloses a method to produce a halo implant region. Assaderaghi in no way solves or

cures the omissions of Yu, described in detail above, with regard to producing the tensile strained finFETs of applicant's invention. In addition, claim 20 depends from claim 12 and contains all the limitations of claim 12 and is allowable for the same reasons as is claim 12.

4. Regarding claim 21 under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Gambino et al. (US 6,689,650 B2) and Literature Digest ("The Highlights of IEDM 2002", vol. 6, March 2003, pp. 1-6), applicant submits Yu in view of Gambino et al. cannot anticipate and render the claims of the present invention obvious because they do not suggest, teach, or yield a tensile strained channel, achieved by the deposition of a silicon channel layer on a SiGe seed layer. Instead, Yu discloses a SiGe channel layer deposited on a silicon seed layer, Gambino et al. is cited as showing the spacers of claim 21, and Literature Digest is cited as showing the salicide step. The combination of Yu in view of Gambino et al. and Literature Digest in no way yields a teaching of applicants' claimed invention, described in detail above, with regard to producing tensile strained finFETs. In addition, claim 21 depends from claim 12 and contains all the limitations of claim 12 and is allowable for the same reasons as is claim 12.

5. Regarding claims 24 and 26, rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to claims 12, 13, 16-19, 22, 23, 25 and 27-30, and further in view of Bae et al. (US 6,633,066 B1), applicant submits Yu in view of Bae et al. cannot anticipate and render the claims of the present invention obvious because they do not suggest, teach, or yield a tensile strained channel, achieved by the deposition of a silicon

channel layer on a SiGe seed layer. Yu discloses a SiGe channel layer deposited on a silicon seed layer and Bae et al. discloses the thickness and composition of silicon germanium. The combination of Yu in view of Bae et al. does not teach or suggest applicants' tensile strained finFET, for the reasons described in detail above. In addition, claims 24 and 26 depend from claim 12 and contain all the limitations of claim 12 and are allowable for the same reasons as is claim 12.

In summary, applicant submits that none of the cited references, singly or in combination, anticipate or render applicants' invention, as defined in amended claim 12, and the claims dependant therefrom, obvious.

Applicants have added new claims 31-41, of which claims 31, 38, and 41 are independent. In each of the new independent claims a method is defined which includes steps in which a relaxed silicon germanium layer substrate region is provided on which an epitaxial silicon layer is deposited and becomes a tensile strained silicon channel layer, due to the lattice mismatch between silicon and silicon germanium. For all the reasons described in detail above, the prior art references cited by the Examiner, either singly or in combination, entirely fail to teach or suggest those recited steps, nor do they achieve applicants' tensile strained finFET. Accordingly, applicants submit that new independent claims 31, 38, and 41, and the claims dependant therefrom, are allowable over the art cited by the Examiner.

This response is accompanied by a Petition for Extension of Time Under 37 C.F.R. §1.136(a) requesting a two-month extension, together with a deposit account authorization for the fee therefore.

In view of the foregoing, applicants request reconsideration of the application, as amended, and submit that the application is now in allowable form and should be passed to issue.

Respectfully submitted,

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